

# TITLE OF THE INVENTION

## SOLID-STATE IMAGE SENSING APPARATUS

### CROSS-REFERENCE TO RELATED APPLICATIONS

This application is based upon and claims the  
5 benefit of priority from the prior Japanese Patent  
Application No. 2003-110436, filed April 15, 2003, the  
entire contents of which are incorporated herein by  
reference.

### BACKGROUND OF THE INVENTION

#### 10 1. Field of the Invention

The present invention relates to a solid-state  
image sensing apparatus which has, e.g., an effective  
signal photoelectric conversion unit and a  
light-shielded reference signal photoelectric  
15 conversion unit to output a black level equivalent  
signal, and corrects the signal output level of the  
effective signal photoelectric conversion unit on the  
basis of the output signal from the reference signal  
photoelectric conversion unit.

#### 20 2. Description of the Related Art

Conventionally, in image sensing using a  
solid-state image sensing apparatus, the pixel output  
variation at the time of reset must be corrected. To  
do this, correlated double sampling (CDS) is executed.  
25 In addition, to make the black level of a video signal  
constant, an error signal (dark current component)  
generated by a dark current must be subtracted from the

video signal. To detect the dark current component, the output signal from a light-shielded pixel (optical black [OB] signal) is referred to.

5 However, in sensing a scene having extremely high luminance as a whole or a scene containing a high-luminance light source such as a spotlight, the OB signal level may vary. If black level correction is done by using the varying OB signal, the video signal may be inappropriate. There is a conventional  
10 technique related to an image sensing apparatus (Jpn. Pat. Appln. KOKAI Publication No. 2002-290841). In this prior art, OB regions are prepared at a plurality of points near the effective pixel region including light-receiving elements which are arrayed on the  
15 light-receiving surface and generate pixel signals. Pixel signals are read out from both regions, thereby preventing any partial decrease in level of the pixel signals after black level correction.

Patent reference 1 above discloses several  
20 techniques for coping with the above-described situation, though none of them can solve the problem practically.

#### BRIEF SUMMARY OF THE INVENTION

The present invention has been made in  
25 consideration of the above technical problem, and has as its object to provide a solid-state image sensing apparatus which can appropriately correct the black

level of a video signal even when a high-luminance state or spotlight exists.

5 In order to achieve the above object, according to an aspect of the present invention, there is provided a solid-state image sensing apparatus comprising an effective signal photoelectric conversion unit to receive object light, and a light-shielded reference signal photoelectric conversion unit to output an optical black level equivalent signal, wherein in  
10 addition to an output from the effective signal photoelectric conversion unit, one of an output from the reference signal photoelectric conversion unit and a predetermined reference voltage is selectively output.

15 Advantages of the invention will be set forth in the description which follows, and in part will be obvious from the description, or may be learned by practice of the invention. Advantages of the invention may be realized and obtained by means of the  
20 instrumentalities and combinations particularly pointed out hereinafter.

#### BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

The accompanying drawings, which are incorporated in and constitute a part of the specification,  
25 illustrate embodiments of the invention, and together with the general description given above and the detailed description of the embodiments given below,

serve to explain the principles of the invention.

FIG. 1 is a view showing the arrangement of a solid-state image sensing apparatus according to the first embodiment of the present invention;

5        FIG. 2A is a timing chart of a read operation for an output signal from a light-shielded pixel unit 1, which is used when the incident light amount is small, in the solid-state image sensing apparatus according to the first embodiment;

10        FIG. 2B is a timing chart of a read operation for a reference signal different from the output signal from the light-shielded pixel unit 1, which is used when very strong light is incident, in the solid-state image sensing apparatus according to the first  
15        embodiment;

FIG. 3 is a view showing the arrangement of a solid-state image sensing apparatus according to the second embodiment of the present invention;

20        FIG. 4A is a timing chart of a read operation for an output signal from a light-shielded pixel unit 1, which is used when the incident light amount is small, in the solid-state image sensing apparatus according to the second embodiment;

25        FIG. 4B is a timing chart of a read operation for a reference signal different from the output signal from the light-shielded pixel unit 1, which is used when very strong light is incident, in the solid-state

image sensing apparatus according to the second embodiment;

FIG. 5 is a view showing the arrangement of a solid-state image sensing apparatus according to the third embodiment of the present invention;

FIG. 6A is a timing chart of a read operation for an output signal from a light-shielded pixel unit 1, which is used when the incident light amount is small, in the solid-state image sensing apparatus according to the third embodiment;

FIG. 6B is a timing chart of a read operation for a reference signal different from the output signal from the light-shielded pixel unit 1, which is used when very strong light is incident, in the solid-state image sensing apparatus according to the third embodiment;

FIG. 7 is a view showing the arrangement of a solid-state image sensing apparatus according to the fourth embodiment of the present invention;

FIG. 8A is a timing chart of a read operation for an output signal from a light-shielded pixel unit 1, which is used when the incident light amount is small, in the solid-state image sensing apparatus according to the fourth embodiment;

FIG. 8B is a timing chart of a read operation for a reference signal different from the output signal from the light-shielded pixel unit 1, which is used

when very strong light is incident, in the solid-state image sensing apparatus according to the fourth embodiment;

5 FIG. 9 is a view showing the arrangement of a solid-state image sensing apparatus according to the fifth embodiment of the present invention;

10 FIG. 10A is a timing chart of a read operation for an output signal from a light-shielded pixel unit 1, which is used when the incident light amount is small, in the solid-state image sensing apparatus according to the fifth embodiment;

15 FIG. 10B is a timing chart of a read operation for a reference signal different from the output signal from the light-shielded pixel unit 1, which is used when very strong light is incident, in the solid-state image sensing apparatus according to the fifth embodiment;

20 FIG. 11 is a view showing the arrangement of a solid-state image sensing apparatus according to the sixth embodiment of the present invention;

25 FIG. 12A is a timing chart of a read operation for an output signal from a light-shielded pixel unit 1, which is used when the incident light amount is small, in the solid-state image sensing apparatus according to the sixth embodiment;

FIG. 12B is a timing chart of a read operation for a reference signal different from the output signal

from the light-shielded pixel unit 1, which is used when very strong light is incident, in the solid-state image sensing apparatus according to the sixth embodiment;

5           FIG. 13A is a timing chart of a read operation for an output signal from a light-shielded pixel unit 1, which is used when the incident light amount is small, in the solid-state image sensing apparatus according to the seventh embodiment;

10           FIG. 13B is a timing chart of a read operation for a reference signal different from the output signal from the light-shielded pixel unit 1, which is used when very strong light is incident, in the solid-state image sensing apparatus according to the seventh  
15           embodiment;

            FIG. 14A is a timing chart of a read operation for an output signal from a light-shielded pixel unit 1, which is used when the incident light amount is small, in the solid-state image sensing apparatus according to  
20           the eighth embodiment;

            FIG. 14B is a timing chart of a read operation for a reference signal different from the output signal from the light-shielded pixel unit 1, which is used when very strong light is incident, in the solid-state  
25           image sensing apparatus according to the eighth embodiment;

            FIG. 15A is a timing chart of a read operation for

an output signal from a light-shielded pixel unit 1, which is used when the incident light amount is small, in the solid-state image sensing apparatus according to the ninth embodiment;

5           FIG. 15B is a timing chart of a read operation for a reference signal different from the output signal from the light-shielded pixel unit 1, which is used when very strong light is incident, in the solid-state image sensing apparatus according to the ninth

10           embodiment;

          FIG. 16 is a block diagram showing the arrangement of a camera according to the 10th embodiment of the present invention;

          FIG. 17 is a view showing an erect object image;

15           FIG. 18 is a flowchart for explaining details of the first operation example of the camera according to the 10th embodiment of the present invention; and

          FIG. 19 is a flowchart for explaining details of the second operation example of the camera according to  
20           the 10th embodiment of the present invention.

#### DETAILED DESCRIPTION OF THE INVENTION

The embodiments of the present invention will be described below with reference to the accompanying drawing.

25           In a solid-state image sensing apparatus according to an embodiment of the present invention, to process CDS and black clamp, a pixel signal or a reference



signal (reference voltage) from light-shielded pixels in a reference signal photoelectric conversion unit (light-shielded pixel unit) can be selectively output. Under a high-luminance condition, a reference level  
5 signal is output in place of a pixel signal from the light-shielded pixels. Each embodiment will be described below in detail based on the above-described characteristic feature.

(First Embodiment)

10 FIG. 1 shows the arrangement of a solid-state image sensing apparatus according to the first embodiment of the present invention. This will be described.

Referring to FIG. 1, reference symbols PIX11 to  
15 PIX33 denote pixels arrayed in a matrix. Of the pixels PIX11 to PIX33, the pixels PIX11 to PIX13 form a light-shielded pixel unit 1. The pixels PIX21 to PIX23 and PIX31 to PIX33 form an effective pixel unit 2. The surfaces of the pixels in the light-shielded pixel unit  
20 1 are covered with a light-shielding film such as an aluminum film.

The light-shielded pixel unit 1 functions as a unit which outputs a signal corresponding to the black level. The effective pixel unit 2 functions as a unit  
25 which receives object light and generates charges.

A vertical scanning circuit 3 sequentially scans row lines H1 to H3 to sequentially read out pixel

signals from the light-shielded pixel unit 1 and effective pixel unit 2. Reference symbols  $\phi V1$  to  $\phi V3$  in the vertical scanning circuit 3 denote row select signals. A noise suppressing circuit 4 suppresses noise components in pixel signals sent from the light-shielded pixel unit 1 and effective pixel unit 2 through vertical signal lines V1 to V3.

Transistors M31 to M33 indicate horizontal select switches to select and read out pixel signals from the noise suppressing circuit 4 (these transistors will be referred to as "horizontal select switches" hereinafter). The gates of the horizontal select switches M31 to M33 are connected to the output terminals of a horizontal scanning circuit 5 for column select signals  $\phi H1$  to  $\phi H3$ .

The horizontal scanning circuit 5 sequentially drives the horizontal select switches M31 to M33. Reference symbols  $\phi H1$  to  $\phi H3$  in the horizontal scanning circuit 5 denote column select signals. An output amplifier 6 amplifies the output signal from the noise suppressing circuit 4, which is sent through the horizontal select switches M31 to M33. Although lines other than the row lines H1 to H3 and vertical signal lines V1 to V3 are also connected to the pixels PIX11 to PIX33, for descriptive convenience, they are not illustrated.

The output signal read operation of the

solid-state image sensing apparatus according to the first embodiment of the present invention will be described below with reference to the timing charts shown in FIGS. 2A and 2B.

5           The read operation for the output signal from the light-shielded pixel unit 1, which is used when the incident light amount is small, in the solid-state image sensing apparatus according to the first embodiment of the present invention will be described first in detail with reference to the timing chart shown in FIG. 2A.

          In the vertical scanning circuit 3, the light-shielded pixel PIX11 and the effective pixels PIX21 and PIX31 are selected by the row select signal  $\phi$  V1 of "H" level. The pixel signals are input to the noise suppressing circuit 4 through the vertical signal lines V1 to V3 so that pixel signals with suppressed noise are obtained. At this time, the pixel signal components of the light-shielded pixel PIX11 and the effective pixels PIX21 and PIX31 are held in CDS1 to CDS3 of the noise suppressing circuit 4. After that, the horizontal scanning circuit 5 sequentially outputs the column select signals  $\phi$  H1 to  $\phi$  H3 of "H" level. Accordingly, the pixel signal components of the light-shielded pixel PIX11 and the effective pixels PIX21 and PIX31, which are stored in the noise suppressing circuit 4, are read out through the

horizontal select switches M31, M32, and M33 in the time-series order and output through the output amplifier 6. In this example, the signal output levels of the effective pixels PIX21 and PIX31 are corrected  
5 on the basis of the signal output level of the light-shielded pixel PIX11.

The read operation for a reference signal different from the output from the light-shielded pixel unit 1, which is used when very strong light such as a  
10 spotlight or sunlight is incident, in the solid-state image sensing apparatus according to the first embodiment of the present invention will be described next in detail with reference to the timing chart shown in FIG. 2B. In the vertical scanning circuit 3, the  
15 light-shielded pixel PIX11 and the effective pixels PIX21 and PIX31 are selected by the row select signal  $\phi$  V1 of "H" level. The pixel signals are input to the noise suppressing circuit 4 through the vertical signal lines V1 to V3.

20 At this time, a reference signal component which is different from the pixel signal component of the light-shielded pixel PIX11 is held in CDS1 of the noise suppressing circuit 4. The pixel signal components of the effective pixels PIX21 and PIX31 are held in CDS2  
25 and CDS3. After that, the horizontal scanning circuit 5 sequentially outputs the column select signals  $\phi$  H1 to  $\phi$  H3 of "H" level. Accordingly, the reference signal

component and the pixel signal components of the effective pixels PIX21 and PIX31, which are stored in the noise suppressing circuit 4, are read out through the horizontal select switches M31, M32, and M33 in the time-series order and output through the output amplifier 6. In this example, the signal output levels of the effective pixels PIX21 and PIX31 are corrected on the basis of the reference signal component different from the pixel signal component of the light-shielded pixel PIX11.

As described above, in the first embodiment, when very strong light such as a spotlight or sunlight is incident, a reference signal component different from the signal components of the light-shielded pixels PIX11 to PIX13 is output. With this arrangement, an image which is not influenced by a black level variation observed in the light-shielded pixels PIX11 to PIX13 can be obtained. In addition, it is unnecessary to output both the output levels of the light-shielded pixels PIX11 to PIX13 and the reference signal level different from the output data of the light-shielded pixels PIX11 to PIX13. For this reason, the time necessary for the read on the entire screen can be shortened.

(Second Embodiment)

FIG. 3 shows the arrangement of a solid-state image sensing apparatus according to the second

embodiment of the present invention. This will be described.

The same reference numerals as in the first embodiment (FIG. 1) denote the same constituent  
5 elements in the second embodiment. Different parts will mainly be described, and a repetitive description will be omitted.

Referring to FIG. 3, reference symbols RS1 to RS3 denote pixel reset lines serving as first row select  
10 lines; TR1 to TR3, PD signal transfer lines serving as second row select lines; and SEL1 to SEL3 denote pixel output select lines serving as third row select lines. Pixel reset signals, PD signal transfer signals, and pixel output select signals sent to these lines are  
15 indicated by  $\phi$ RS1 to  $\phi$ RS3,  $\phi$ TR1 to  $\phi$ TR3, and  $\phi$ SEL1 to  $\phi$ SEL3, respectively.

A pixel power supply line 7 supplies a power to reset MOS transistors M211 to M233 and amplification MOS transistors M311 to M333.

20 Pixels PIX11 to PIX33 which form a light-shielded pixel unit 1 and an effective pixel unit 2 include photodiodes D11 to D33, transfer MOS transistors M111 to M133, the reset MOS transistors M211 to M233, the amplification MOS transistors M311 to M333, and select  
25 MOS transistors M411 to M433, respectively. The transfer MOS transistors M111 to M133 cause the photodiodes D11 to D33 to transfer charges and read

them out. The reset MOS transistors M211 to M233 reset the transferred charges. The amplification MOS transistors M311 to M333 amplify the charges in the photodiodes D11 to D33. The select MOS transistors  
5 M411 to M433 select rows.

More specifically, the gates of the reset MOS transistors M211, M221, and M231 are connected to the pixel reset line RS1. The gates of the reset MOS transistors M212, M222, and M232 are connected to the  
10 pixel reset line RS2. The gates of the reset MOS transistors M213, M223, and M233 are connected to the pixel reset line RS3.

The gates of the transfer MOS transistors M111, M121, and M131 are connected to the PD signal transfer line TR1. The gates of the transfer MOS transistors  
15 M112, M122, and M132 are connected to the PD signal transfer line TR2. The gates of the transfer MOS transistors M113, M123, and M133 are connected to the PD signal transfer line TR3.

The gates of the select MOS transistors M411, M421, and M431 are connected to the pixel output select line SEL1. The gates of the select MOS transistors  
20 M412, M422, and M432 are connected to the pixel output select line SEL2. The gates of the select MOS transistors M413, M423, and M433 are connected to the  
25 pixel output select line SEL3.

A vertical scanning circuit 3 outputs pixel reset

signals  $\phi$ RS1 to  $\phi$ RS3, PD signal transfer signals  $\phi$ TR1 to  $\phi$ TR3, and pixel output select signals  $\phi$ SEL1 to  $\phi$ SEL3. The above-described units are driven and controlled by these signals.

5           Reference symbols V1 to V3 denote vertical signal lines to extract the output signals from the amplification MOS transistors M311 to M313, M321 to M323, and M331 to M333. Reference symbols I41 to I43 denote current sources to bias the vertical signal  
10       lines V1 to V3.

          A noise suppressing circuit 4 includes clamp capacitors CCL1 to CCL3 connected to the vertical signal lines V1 to V3, sample-and-hold switches M11 to M13, clamp switches M21 to M23, and sample-and-hold  
15       capacitors CSH1 to CSH3.

          The clamp capacitors CCL1 to CCL3 store the reset levels of the vertical signal lines V1 to V3. The sample-and-hold capacitors CSH1 to CSH3 store the amplification components of the vertical signal lines  
20       V1 to V3.

          The sample-and-hold switches M11 to M13 transmit the signals of the vertical signal lines V1 to V3 to the sample-and-hold capacitors CSH1 to CSH3. The gates of the sample-and-hold switches M11 to M13 are  
25       connected to a sample-and-hold control line SH and driven and controlled by a sample-and-hold control signal.



Each of the clamp switches M21 to M23 sets the terminal potential of one of a corresponding one of the clamp capacitors CCL1 to CCL3 and a corresponding one of the sample-and-hold capacitors CSH1 to CSH3 to a reference potential supplied from a clamp voltage line 8. The gate of the clamp switch M21 is connected to a clamp control line CL2 and driven and controlled by a clamp control signal  $\phi$ CL2. The gates of the clamp switches M22 and M23 are connected to a clamp control line CL1 and driven and controlled by a clamp control signal  $\phi$ CL1.

The connection points between the sample-and-hold capacitors CSH1 to CSH3 and the clamp switches M21 to M23 are connected to an output amplifier 6 through horizontal select switches M31 to M33. The gates of the horizontal select switches M31 to M33 are connected to the output terminals of a horizontal scanning circuit 5 for column select signals  $\phi$ H1 to  $\phi$ H3.

The output signal read operation of the solid-state image sensing apparatus according to the second embodiment of the present invention will be described below with reference to the timing charts shown in FIGS. 4A and 4B.

The read operation for the output signal from the light-shielded pixel unit 1, which is used when the incident light amount is small, in the solid-state image sensing apparatus according to the second

embodiment of the present invention will be described first in detail with reference to the timing chart shown in FIG. 4A.

When light becomes incident on the photodiodes D11 to D33 of the pixels PIX11 to PIX33, the photodiodes D11 to D33 generate and store optical signal charges. The stored pixel signals are sequentially read out to the vertical signal lines V1 to V3 for the respective rows while being vertically scanned by the vertical scanning circuit 3.

The operation in selecting the pixels of the first row will be described.

First, the pixel output select signal  $\phi\text{SEL1}$  is set to "H" level to connect the amplification MOS transistors M311, M321, and M331 to the vertical signal lines V1 to V3 and current sources I41 to I43 through the row select MOS transistors M411, M421, and M431. Before the read of optical signal charges from the photodiodes D11 to D31, the pixel reset signal  $\phi\text{RS1}$  is set to "H" level to reset the gates of the amplification MOS transistors M311, M321, and M331 to the pixel power supply through the reset MOS transistors M211, M221, and M231.

In addition, both a sample-and-hold control signal  $\phi\text{SH}$  and the clamp control signals  $\phi\text{CL1}$  and  $\phi\text{CL2}$  are set to "H" level to initialize the terminal potentials of the clamp capacitors CCL1 to CCL3 and

sample-and-hold capacitors CSH1 to CSH3 to the potential of the clamp voltage line 8 through the sample-and-hold switches M11 to M13 and clamp switches M21 to M23. Next, the pixel reset signal  $\phi_{RS1}$  is  
5 returned to "L" level to disconnect the pixel power supply line 7 from the gates of the amplification MOS transistors M311, M321, and M331. At this timing, the reset signal components of the vertical signal lines V1 to V3 are stored in the clamp capacitors CCL1 to CCL3.

10 With this operation, the reset signal components containing reset noise and element variations in the amplification MOS transistors M311, M321, and M331 are stored in the clamp capacitors CCL1 to CCL3. After the end of signal storage in the clamp capacitors CCL1 to  
15 CCL3, the clamp control signals  $\phi_{CL1}$  and  $\phi_{CL2}$  are set to "L" level to set the connection points between the sample-and-hold capacitors CSH1 to CSH3 and the clamp switches M21 to M23 in a high-impedance state.

After that, the PD signal transfer signal  $\phi_{TR1}$  is  
20 set to "H" level to transfer the optical signal charges in the photodiodes D11 to D31 to the gates of the amplification MOS transistors M311, M321, and M331 through the transfer MOS transistors M111, M121, and M131. After the end of transfer, the PD signal  
25 transfer signal  $\phi_{TR1}$  is returned to "L" level to disconnect the photodiodes D11 to D31 from the gates of the amplification MOS transistors M311, M321, and M331.

At this timing, potential variations as the voltage differences between the reset signal components and the optical signal components, which appear on the vertical signal lines V1 to V3, are stored in the sample-and-hold capacitors CSH1 to CSH3 through the clamp capacitors CCL1 to CCL3 and sample-and-hold switches M11 to M13. After that, when the sample-and-hold control signal  $\phi_{SH}$  is returned to "L" level, the optical signal components of all pixel cells of the light-shielded pixel PIX11 and effective pixels PIX21 and PIX31 are held in the sample-and-hold capacitors CSH1 to CSH3. The column select signals  $\phi_{H1}$  to  $\phi_{H3}$  from the horizontal scanning circuit 5 are sequentially set to "H" level. Accordingly, the voltages held in the sample-and-hold capacitors CSH1 to CSH3 are read out through the horizontal select switches M31 to M33 and sequentially output through the output amplifier 6.

The read of the pixel cells connected to the first row is thus completed. In the second embodiment, the signal output levels of the effective pixels PIX21 and PIX31 are corrected on the basis of the signal output level of the light-shielded pixel PIX11. In the same way as described above, the signals of the pixel cells connected to the second and subsequent rows are sequentially read out in accordance with the row select signals from the vertical scanning circuit 3 so that

the read of all pixel cells is ended.

The read operation for a reference signal different from the output from the light-shielded pixel unit 1, which is used when very strong light such as a spotlight or sunlight is incident, in the solid-state image sensing apparatus according to the second embodiment of the present invention will be described next in detail with reference to the timing chart shown in FIG. 4B. The operation until reset signal components are stored in the clamp capacitors CCL1 to CCL3 is the same as in FIG. 4A, and repetitive description will be omitted.

After the end of storage in the clamp capacitors CCL1 to CCL3, the clamp control signal  $\phi_{CL1}$  is set to "L" level to set the connection points between the sample-and-hold capacitors CSH2 and CSH3 and the clamp switches M22 and M23 in a high-impedance state. On the other hand, the clamp control signal  $\phi_{CL1}$  holds "H" level. The terminal potentials of the clamp capacitor CCL1 and sample-and-hold capacitor CSH1 are still fixed to the potential of the clamp voltage line 8. After that, the PD signal transfer signal  $\phi_{TR1}$  is set to "H" level to transfer the optical signal charges in the photodiodes D11 to D31 to the gates of the amplification MOS transistors M311, M321, and M331 through the transfer MOS transistors M111, M121, and M131.

After the end of transfer, the PD signal transfer signal  $\phi_{TR1}$  is returned to "L" level to disconnect the photodiodes D11 to D31 from the gates of the amplification MOS transistors M311, M321, and M331.

5           At this time, potential variations as the voltage differences between the reset signal components and the optical signal components, which appear on the vertical signal lines V2 and V3, are stored in the sample-and-hold capacitors CSH2 and CSH3 through the  
10       clamp capacitors CCL2 and CCL3 and sample-and-hold switches M12 and M13. On the other hand, the clamp control signal  $\phi_{CL2}$  holds "H" level. The terminal potentials of the clamp capacitor CCL1 and sample-and-hold capacitor CSH1 are still fixed to the  
15       potential of the clamp voltage line 8. After that, the sample-and-hold control signal  $\phi_{SH}$  is returned to "L" level, and the clamp control signal  $\phi_{CL2}$  is set to "L" level. Accordingly, the clamp voltage level as the potential of the clamp voltage line 8 is held in the  
20       sample-and-hold capacitor CSH1. The optical signal components of the effective pixels PIX21 and PIX31 are held in the sample-and-hold capacitors CSH2 and CSH3.

          Finally, the column select signals  $\phi_{H1}$  to  $\phi_{H3}$  from the horizontal scanning circuit 5 are sequentially  
25       set to "H" level. Accordingly, the voltages held in the sample-and-hold capacitors CSH1 to CSH3 are read out through the horizontal select switches M31 to M33

and sequentially output through the output amplifier 6. The read of the pixel cells connected to the first row is thus completed.

5 In the second embodiment, the signal output levels of the effective pixels PIX21 and PIX31 are corrected on the basis of the clamp voltage level as the potential of the clamp voltage line 8. In the same way as described above, the signals of the pixel cells connected to the second and subsequent rows are  
10 sequentially read out in accordance with the row select signals from the vertical scanning circuit 3 so that the read of all pixel cells is ended.

As described above, in the second embodiment, when very strong light such as a spotlight or sunlight is  
15 incident, a reference signal level different from the signal components of the light-shielded pixels PIX11 to PIX13 is output. With this arrangement, an image which is not influenced by a black level variation observed in the light-shielded pixels PIX11 to PIX13 can be  
20 obtained. In addition, one control line for the noise suppressing circuit 4 is added to change the drive timing. This change makes it possible to select whether the signal components from the light-shielded pixels PIX11 to PIX13 or the reference signal level is  
25 to be output. Hence, the increase in chip area can be minimized. Furthermore, it is unnecessary to output both the output levels of the light-shielded pixels

PIX11 to PIX13 and the reference signal level different from the output data of the light-shielded pixels PIX11 to PIX13. For this reason, the time necessary for the read on the entire screen can be shortened.

5 (Third Embodiment)

FIG. 5 shows the arrangement of a solid-state image sensing apparatus according to the third embodiment of the present invention. This will be described.

10 The same reference numerals as in the second embodiment (FIG. 3) denote the same constituent elements in the third embodiment. Different parts will mainly be described, and repetitive description will be omitted.

15 Referring to FIG. 5, the solid-state image sensing apparatus according to the third embodiment employs a different driving method for a noise suppressing circuit 4.

20 In the above-described second embodiment, all the gates of the sample-and-hold switches M11 to M13 are connected to the sample-and-hold control line SH. In the third embodiment, the gate of a sample-and-hold switch M11 is connected to a sample-and-hold control line SH2. The gates of sample-and-hold switches M12  
25 and M13 are connected to a sample-and-hold control line SH1.

That is, in the third embodiment, the



sample-and-hold switch M11 is driven and controlled by a sample-and-hold control signal  $\phi SH2$ . The sample-and-hold switches M12 and M13 are driven and controlled by a sample-and-hold control signal  $\phi SH1$ .

5           In addition, in the above-described second embodiment, the gate of the clamp switch M21 is connected to the clamp control line CL2, and the gates of the clamp switches M22 and M23 are connected to the clamp control line CL1. In the third embodiment, the  
10           gates of clamp switches M21 to M23 are connected to a clamp control line CL. That is, all the clamp switches M21 to M23 are driven and controlled by a clamp control signal  $\phi CL$ . The remaining parts are the same as in FIG. 3.

15           The read operation for the output signal from a light-shielded pixel unit 1, which is used when the incident light amount is small, in the solid-state image sensing apparatus according to the third embodiment of the present invention will be described  
20           first with reference to the timing chart shown in FIG. 6A. The sample-and-hold control signals  $\phi SH1$  and  $\phi SH2$  are driven at the same timing as that of the sample-and-hold control signal  $\phi SH$  in FIG. 4A. The clamp control signal  $\phi CL$  is driven at the same timing  
25           as that of the clamp control signal  $\phi CL1$  in FIG. 4A. In this case, the drive timing is the same as in FIG. 4(A), and repetitive description will be omitted.

The read operation for a reference signal different from the output from the light-shielded pixel unit 1, which is used when very strong light such as a spotlight or sunlight is incident, in the solid-state image sensing apparatus according to the third  
5 embodiment of the present invention will be described next in detail with reference to the timing chart shown in FIG. 6B. The operation until reset signal components are stored in clamp capacitors CCL1 to CCL3  
10 is the same as in FIG. 4A, and a repetitive description will be omitted.

After the end of storage in the clamp capacitors CCL1 to CCL3, the clamp control signal  $\phi_{CL}$  is set to "L" level to set the connection points between  
15 sample-and-hold capacitors CSH1 to CSH3 and the clamp switches M21 to M23 in a high-impedance state. Subsequently, the sample-and-hold control signal  $\phi_{SH2}$  is returned to "L" level to cause the sample-and-hold capacitor CSH1 to hold the clamp voltage level as the  
20 potential of a clamp voltage line 8.

After that, a PD signal transfer signal  $\phi_{TR1}$  is set to "H" level to transfer optical signal charges in photodiodes D11 to D31 to the gates of amplification MOS transistors M311, M321, and M331 through transfer  
25 MOS transistors M111, M121, and M131. After the end of transfer, the PD signal transfer signal  $\phi_{TR1}$  is returned to "L" level to disconnect the photodiodes D11

to D31 from the gates of the amplification MOS transistors M311, M321, and M331.

At this timing, potential variations as the voltage differences between the reset signal components and the optical signal components, which appear on vertical signal lines V2 and V3, are stored in the sample-and-hold capacitors CSH2 and CSH3 through clamp capacitors CCL2 and CCL3 and sample-and-hold switches M12 and M13.

On the other hand, the sample-and-hold capacitor CSH1 continuously holds the clamp voltage level as the potential of the clamp voltage line 8. After that, the sample-and-hold control signal  $\phi_{SH1}$  is returned to "L" level. Accordingly, the clamp voltage level as the potential of the clamp voltage line 8 is held in the sample-and-hold capacitor CSH1. The optical signal components of effective pixels PIX21 and PIX31 are held in the sample-and-hold capacitors CSH2 and CSH3.

Finally, column select signals  $\phi_{H1}$  to  $\phi_{H3}$  from a horizontal scanning circuit 5 are sequentially set to "H" level. Accordingly, the voltages held in the sample-and-hold capacitors CSH1 to CSH3 are read out through horizontal select switches M31 to M33 and sequentially output through an output amplifier 6. The read of the pixel cells connected to the first row is thus completed.

In the third embodiment, the signal output levels

of the effective pixels PIX21 and PIX31 are corrected on the basis of the clamp voltage level as the potential of the clamp voltage line 8. In the same way as described above, the signals of the pixel cells  
5 connected to the second and subsequent rows are sequentially read out in accordance with the row select signals from a vertical scanning circuit 3 so that the read of all pixel cells is ended.

As described above, in the third embodiment, when  
10 very strong light such as a spotlight or sunlight is incident, a reference signal level different from the signal components of light-shielded pixels PIX11 to PIX13 is output. With this arrangement, an image which is not influenced by a black level variation observed  
15 in the light-shielded pixels PIX11 to PIX13 can be obtained. In addition, one control line for a noise suppressing circuit 4 is added to change the drive timing. This change makes it possible to select whether the signal components from the light-shielded  
20 pixels PIX11 to PIX13 or the reference signal level is to be output. Hence, the increase in chip area can be minimized. Furthermore, it is unnecessary to output both the output levels of the light-shielded pixels PIX11 to PIX13 and the reference signal level different  
25 from the output data of the light-shielded pixels PIX11 to PIX13. For this reason, the time necessary for the read on the entire screen can be shortened.

(Fourth Embodiment)

FIG. 7 shows the arrangement of a solid-state image sensing apparatus according to the fourth embodiment of the present invention. This will be described.

The same reference numerals as in the second embodiment (FIG. 3) denote the same constituent elements in the fourth embodiment. Different parts will mainly be described, and repetitive description will be omitted.

Referring to FIG. 7, the solid-state image sensing apparatus according to the fourth embodiment employs a different driving method for a noise suppressing circuit 4. More specifically, vertical signal lines V1 to V3 have reset signal switches M41 to M43, optical signal switches M51 to M53, reset signal capacitors CSHR1 to CSHR3, and optical signal capacitors CSHS1 to CSHS3, respectively. The reset signal capacitors CSHR1 to CSHR3 store the reset levels of the vertical signal lines V1 to V3. The optical signal capacitors CSHS1 to CSHS3 store the optical signal levels of the vertical signal lines V1 to V3. The gates of the reset signal switches M41 to M43 are connected to a reset signal sample control line SHR and driven and controlled by a reset signal sample control signal  $\phi$  SHR. The gate of the optical signal switch M51 is connected to an optical signal sample control line SHS2 and driven and

controlled by an optical signal sample control signal  $\phi$  SHS2. The gates of the optical signal switches M52 and M53 are connected to an optical signal sample control line SHS1 and driven and controlled by an optical  
5 signal sample control signal  $\phi$  SHS1. Horizontal select switches M61 to M63 and M71 to M73 read out signals held in the reset signal capacitors CSHR1 to CSHR3 and optical signal capacitors CSHS1 to CSHS3. A differential circuit 9 obtains the difference between a  
10 reset component and an optical signal component. The remaining parts are the same as in FIG. 3.

The read operation for the output signal from a light-shielded pixel unit 1, which is used when the incident light amount is small, in the solid-state  
15 image sensing apparatus according to the fourth embodiment of the present invention will be described first with reference to the timing chart shown in FIG. 8A.

When light becomes incident on photodiodes D11 to D33 of pixels PIX11 to PIX33, the photodiodes D11 to  
20 D33 generate and store optical signal charges. The stored pixel signals are sequentially read out to the vertical signal lines V1 to V3 for the respective rows while being vertically scanned by a vertical scanning  
25 circuit 3.

The operation in selecting the pixels of the first row will be described.

First, a pixel output select signal  $\phi\text{SEL1}$  is set to "H" level to connect amplification MOS transistors M311, M321, and M331 to the vertical signal lines V1 to V3 and current sources I41 to I43 through row select  
5 MOS transistors M411, M421, and M431. Before the read of optical signal charges from the photodiodes D11 to D31, a pixel reset signal  $\phi\text{RS1}$  is set to "H" level to reset the gates of the amplification MOS transistors M311, M321, and M331 to the pixel power supply through  
10 reset MOS transistors M211, M221, and M231. Next, the pixel reset signal  $\phi\text{RS1}$  is returned to "L" level to disconnect a pixel power supply line 7 from the gates of the amplification MOS transistors M311, M321, and M331.

15 Subsequently, the reset signal sample control signal  $\phi\text{SHR}$  is set to "H" level to store the reset signal components of the vertical signal lines V1 to V3 in the reset signal capacitors CSHR1 to CSHR3 through the reset signal switches M41 to M43. After the end of  
20 storage in the reset signal capacitors CSHR1 to CSHR3, the reset signal sample control signal  $\phi\text{SHR}$  is returned to "L" level to cause the reset signal capacitors CSHR1 to CSHR3 to hold the stored reset signal components.

After that, a PD signal transfer signal  $\phi\text{TR1}$  is  
25 set to "H" level to transfer the optical signal charges in the photodiodes D11 to D31 to the gates of the amplification MOS transistors M311, M321, and M331

through transfer MOS transistors M111, M121, and M131. After the end of transfer, the PD signal transfer signal  $\phi_{TR1}$  is returned to "L" level to disconnect the photodiodes D11 to D31 from the gates of the amplification MOS transistors M311, M321, and M331.

Subsequently, the optical signal sample control signals  $\phi_{SHS1}$  and  $\phi_{SHS2}$  are set to "H" level to store the optical signal components of the vertical signal lines V1 to V3 in the optical signal capacitors CSHS1 to CSHS3 through the optical signal switches M51 to M53. After the end of storage in the optical signal capacitors CSHS1 to CSHS3, the optical signal sample control signals  $\phi_{SHS1}$  and  $\phi_{SHS2}$  are returned to "L" level to cause the optical signal capacitors CSHS1 to CSHS3 to hold the stored optical signal components. Finally, column select signals  $\phi_{H1}$  to  $\phi_{H3}$  from a horizontal scanning circuit 5 are sequentially set to "H" level. Accordingly, the voltages held in the reset signal capacitors CSHR1 to CSHR3 and optical signal capacitors CSHS1 to CSHS3 are read out to the differential circuit 9 through the horizontal select switches M61 to M63 and M71 to M73. The differential circuit 9 obtains the difference between each reset signal component and a corresponding optical signal component and sequentially outputs the difference to a sensor output line OUT.

The read of the pixel cells connected to the first



row is thus completed. In the fourth embodiment, the signal output levels of the effective pixels PIX21 and PIX31 are corrected on the basis of the signal output level of the light-shielded pixel PIX11. In the same way as described above, the signals of the pixel cells connected to the second and subsequent rows are sequentially read out in accordance with the signals from the vertical scanning circuit 3 so that the read of all pixel cells is ended.

The read operation for a reference signal different from the output from the light-shielded pixel unit 1, which is used when very strong light such as a spotlight or sunlight is incident, in the solid-state image sensing apparatus according to the fourth embodiment of the present invention will be described next in detail with reference to the timing chart shown in FIG. 8B. First, the pixel output select signal  $\phi_{SEL1}$  is set to "H" level to connect the amplification MOS transistors M311, M321, and M331 to the vertical signal lines V1 to V3 and the current sources I41 to I43 through the row select MOS transistors M411, M421, and M431.

Before the read of optical signal charges from the photodiodes D11 to D31, the pixel reset signal  $\phi_{RS1}$  is set to "H" level to reset the gates of the amplification MOS transistors M311, M321, and M331 to the pixel power supply through the reset MOS

transistors M211, M221, and M231.

Next, the pixel reset signal  $\phi RS1$  is returned to "L" level to disconnect the pixel power supply line 7 from the gates of the amplification MOS transistors

5 M311, M321, and M331. Subsequently, the reset signal sample control signal  $\phi SHR$  is set to "H" level to store the reset signal components of the vertical signal lines V1 to V3 in the reset signal capacitors CSHR1 to CSHR3 through the reset signal switches M41 to M43.

10 Simultaneously, the optical signal sample control signal  $\phi SHS2$  is set to "H" level to store the reset signal component of the vertical signal line V1 in the optical signal capacitor CSHS1 through the optical signal switch M51. After the end of storage in the  
15 reset signal capacitors CSHR1 to CSHR3 and storage in optical signal capacitors CSHS1 to CSHS3, the reset signal sample control signal  $\phi SHR$  and optical signal sample control signal  $\phi SHS2$  are returned to "L" level to cause the reset signal capacitors CSHR1 to CSHR3 and  
20 optical signal capacitor CSHS1 to hold the stored reset signal components.

After that, the PD signal transfer signal  $\phi TR1$  is set to "H" level to transfer the optical signal charges in the photodiodes D11 to D31 to the gates of the  
25 amplification MOS transistors M311, M321, and M331 through the transfer MOS transistors M111, M121, and M131. After the end of transfer, the PD signal

transfer signal  $\phi_{TR1}$  is returned to "L" level to  
disconnect the photodiodes D11 to D31 from the gates of  
the amplification MOS transistors M311, M321, and M331.  
Subsequently, the optical signal sample control signal  
5  $\phi_{SHS1}$  is set to "H" level to store the optical signal  
components of the vertical signal lines V2 and V3 in  
the optical signal capacitors CSHS2 and CSHS3 through  
the optical signal switches M52 and M53.

After the end of storage in the optical signal  
10 capacitors CSHS2 and CSHS3, the optical signal sample  
control signal  $\phi_{SHS1}$  is returned to "L" level to cause  
the optical signal capacitors CSHS2 and CSHS3 to hold  
the stored optical signal components. Finally, the  
column select signals  $\phi_{H1}$  to  $\phi_{H3}$  from the horizontal  
15 scanning circuit 5 are sequentially set to "H" level.  
Accordingly, the voltages held in the reset signal  
capacitors CSHR1 to CSHR3 and optical signal capacitors  
CSHS1 to CSHS3 are read out to the differential circuit  
9 through the horizontal select switches M61 to M63 and  
20 M71 to M73. The differential circuit 9 obtains the  
difference between each reset signal component and a  
corresponding optical signal component and sequentially  
outputs the difference to the sensor output line OUT.

The read of the pixel cells connected to the first  
25 row is thus completed.

In the fourth embodiment, both the reset signal  
capacitor CSHR1 and the optical signal capacitor CSHS1

hold the reset signal components. For this reason, the output from the differential circuit 9 is zero. The signal output levels of the effective pixels PIX21 and PIX31 are corrected on the basis of the zero output  
5 from the differential circuit 9. In the same way as described above, the signals of the pixel cells connected to the second and subsequent rows are sequentially read out in accordance with the signals from the vertical scanning circuit 3 so that the read  
10 of all pixel cells is ended.

As described above, in the fourth embodiment, when very strong light such as a spotlight or sunlight is incident, a reference signal level different from the signal components of the light-shielded pixels PIX11 to PIX13 is output. With this arrangement, an image which  
15 is not influenced by a black level variation observed in the light-shielded pixels PIX11 to PIX13 can be obtained. In addition, one control line for the noise suppressing circuit 4 is added to change the drive  
20 timing. This change makes it possible to select whether the signal components from the light-shielded pixels PIX11 to PIX13 or the reference signal level is to be output. Hence, the increase in chip area can be minimized. Furthermore, it is unnecessary to output  
25 both the output levels of the light-shielded pixels PIX11 to PIX13 and the reference signal level different from the output data of the light-shielded pixels PIX11

to PIX13. For this reason, the time necessary for the read on the entire screen can be shortened. In addition, any degradation in characteristic due to power supply noise, GND noise, common mode noise component, and the like can be suppressed by executing differential processing.

(Fifth Embodiment)

FIG. 9 shows the arrangement of a solid-state image sensing apparatus according to the fifth embodiment of the present invention. This will be described.

The same reference numerals as in the second embodiment (FIG. 3) denote the same constituent elements in the fifth embodiment. Different parts will mainly be described, and repetitive description will be omitted.

Referring to FIG. 9, as a characteristic feature of the solid-state image sensing apparatus according to the fifth embodiment, a light-shielded pixel power supply line 10 which supplies a power to a light-shielded pixel unit 1 is newly added independently of an effective pixel power supply line 7 which supplies a power to an effective pixel unit 2. In the second embodiment, the gate of the clamp switch M21 is connected to the clamp control line CL2, and the gates of the clamp switches M22 and M23 are connected to the clamp control line CL1. In the fifth

embodiment, the gates of clamp switches M21 to M23 of a noise suppressing circuit 4 are connected to a clamp control line CL and driven and controlled by a clamp control signal  $\phi CL$ .

5           The read operation for the output signal from the light-shielded pixel unit 1, which is used when the incident light amount is small, in the solid-state image sensing apparatus according to the fifth embodiment of the present invention will be described  
10 first with reference to the timing chart shown in FIG. 10A. The light-shielded pixel power supply line 10 and effective pixel power supply line 7 are set to a common potential. A sample-and-hold control signal  $\phi SH$  is set to "H" level at the same timing as that of the  
15 sample-and-hold control signal  $\phi SH$  in FIG. 4A. The clamp control signal  $\phi CL$  is set to "H" level at the same timing as that of the clamp control signal  $\phi CL1$  in FIG. 4A. In this case, the drive timing is the same as in FIG. 4A, and repetitive description will be omitted.

20           The read operation for a reference signal different from the output from the light-shielded pixel unit 1, which is used when very strong light such as a spotlight or sunlight is incident, in the solid-state image sensing apparatus according to the fifth  
25 embodiment of the present invention will be described next in detail with reference to the timing chart shown in FIG. 10B. In this case, the same driving operation

as in FIG. 10A (FIG. 4A) is performed except that the light-shielded pixel power supply line 10 is fixed to the GND potential.

First, a pixel output select signal  $\phi_{SEL1}$  is set to "H" level to connect amplification MOS transistors M321 and M331 to vertical signal lines V2 and V3 and current sources I42 and I43 through row select MOS transistors M421 and M431. On the other hand, a vertical signal line V1 is fixed to GND because there is no current path flowing to a pixel current source I41. Before the read of optical signal charges from photodiodes D11 to D31, a pixel reset signal  $\phi_{RS1}$  is set to "H" level to reset the gates of the amplification MOS transistors M321 and M331 to the effective pixel power supply line 7 through reset MOS transistors M221 and M231.

On the other hand, the gate potential of an amplification MOS transistor M311 is set to the GND potential. The potential is fixed to GND because the light-shielded pixel power supply line 10 is disconnected from the vertical signal line V1, and there is no current path flowing to the pixel current source I41. In addition, the sample-and-hold control signal  $\phi_{SH}$  and the clamp control signal  $\phi_{CL}$  are set to "H" level to initialize the terminal potentials of clamp capacitors CCL1 to CCL3 and sample-and-hold capacitors CSH1 to CSH3 to the potential of a clamp

voltage line 8 through sample-and-hold switches M11 to M13 and clamp switches M21 to M23.

Next, the pixel reset signal  $\phi_{RS1}$  is returned to "L" level to disconnect the effective pixel power supply line 7 from the gates of the amplification MOS transistors M311, M321, and M331. At this time, the reset signal components of the vertical signal lines V2 and V3 are stored in the clamp capacitors CCL2 and CCL3. The GND component of the vertical signal line V1 is stored in the clamp capacitor CCL1. With this operation, the reset signal components containing reset noise and element variations in the amplification MOS transistors M311, M321, and M331 are stored in the clamp capacitors CCL2 and CCL3. After the end of storage in the clamp capacitors CCL1 to CCL3, the clamp control signal  $\phi_{CL}$  is set to "L" level to set the connection points between the sample-and-hold capacitors CSH1 to CSH3 and the clamp switches M21 to M23 in a high-impedance state.

After that, a PD signal transfer signal  $\phi_{TR1}$  is set to "H" level to transfer the optical signal charges in the photodiodes D21 and D31 to the gates of the amplification MOS transistors M321 and M331 through the transfer MOS transistors M121 and M131. On the other hand, the optical signal charges in the photodiode D11 cannot be transferred because the gate potential of the amplification MOS transistor M311 is GND. The



potential remains almost GND. After the end of transfer, the PD signal transfer signal  $\phi_{TR1}$  is returned to "L" level again to disconnect the photodiodes D11 to D31 from the gates of the amplification MOS transistors M311, M321, and M331.

At this time, potential variations as the voltage differences between the reset signal components and the optical signal components, which appear on the vertical signal lines V2 and V3, are stored in the sample-and-hold capacitors CSH2 and CSH3 through the clamp capacitors CCL2 and CCL3 and sample-and-hold switches M12 and M13. On the other hand, the vertical signal line V1 is kept at GND and does not vary. The sample-and-hold capacitor CSH1 holds the potential of the clamp voltage line 8.

After that, when the sample-and-hold control signal  $\phi_{SH}$  is returned to "L" level again, the clamp voltage level as the potential of the clamp voltage line 8 is held in the sample-and-hold capacitor CSH1, and the optical signal components of effective pixels PIX21 and PIX31 are held in the sample-and-hold capacitors CSH2 and CSH3. Finally, column select signals  $\phi_{H1}$  to  $\phi_{H3}$  from a horizontal scanning circuit are sequentially set to "H" level. Accordingly, the voltages held in the sample-and-hold capacitors CSH1 to CSH3 are read out through horizontal select switches M31 to M33 and sequentially output through an output

amplifier 6. The read of the pixel cells connected to the first row is thus completed.

5 In the fifth embodiment, the signal output levels of the effective pixels PIX21 and PIX31 are corrected on the basis of the clamp voltage level as the potential of the clamp voltage line 8. In the same way as described above, the signals of the pixel cells connected to the second and subsequent rows are sequentially read out in accordance with row select  
10 signals from a vertical scanning circuit 3 so that the read of all pixel cells is ended.

As described above, in the fifth embodiment, when very strong light such as a spotlight or sunlight is incident, a reference signal level different from the  
15 signal components of light-shielded pixels PIX11 to PIX13 is output. With this arrangement, an image which is not influenced by a black level variation observed in the light-shielded pixels PIX11 to PIX13 can be obtained. In addition, a pixel power supply for the  
20 light-shielded pixel unit 1 is newly added to change the drive timing. This change makes it possible to select whether the signal components from the light-shielded pixels PIX11 to PIX13 or the reference signal level is to be output. Hence, the increase in  
25 chip area can be minimized. Furthermore, it is unnecessary to output both the output levels of the light-shielded pixels PIX11 to PIX13 and the reference

signal level different from the output data of the light-shielded pixels. For this reason, the time necessary for the read on the entire screen can be shortened.

5 (Sixth Embodiment)

FIG. 11 shows the arrangement of a solid-state image sensing apparatus according to the sixth embodiment of the present invention. This will be described.

10 The same reference numerals as in the fifth embodiment (FIG. 9) denote the same constituent elements in the sixth embodiment. Different parts will mainly be described, and repetitive description will be omitted.

15 The solid-state image sensing apparatus according to the sixth embodiment is based on the arrangement shown in FIG. 9 but has a noise suppressing circuit 4 having a different structure. The structure of the noise suppressing circuit 4 is basically the same as in  
20 FIG. 7 except the following points.

In the above-described structure shown in FIG. 7, the gate of the photodetection switch M51 is connected to the optical signal sample control line SHS2 and driven and controlled by the optical signal sample  
25 control signal  $\phi$ SHS2. The gates of the photodetection switches M52 and M53 are connected to the optical signal sample control line SHS1 and driven and

controlled by the optical signal sample control signal  $\phi$ SHS1. In the sixth embodiment, the gates of photodetection switches M51 to M53 are connected to an optical signal sample control line SHS and driven and controlled by an optical signal sample control signal  $\phi$ SHS. The remaining parts are the same as in FIGS. 7 and 9, and detailed description thereof will be omitted.

The read operation for the output signal from a light-shielded pixel unit 1, which is used when the incident light amount is small, in the solid-state image sensing apparatus according to the sixth embodiment of the present invention will be described first with reference to the timing chart shown in FIG. 12A. A light-shielded pixel power supply line 10 and an effective pixel power supply line 7 are set to a common potential. A reset signal sample control signal  $\phi$ SHS is set to "H" level at the same timing as that of the reset signal sample control signal  $\phi$ SHS1 in FIG. 8A. In this case, the drive timing is the same as in FIG. 8A, and detailed description thereof will be omitted.

The read operation for a reference signal different from the output from the light-shielded pixel unit 1, which is used when very strong light such as a spotlight or sunlight is incident, in the solid-state image sensing apparatus according to the sixth

embodiment of the present invention will be described next in detail with reference to the timing chart shown in FIG. 12B. In this case, the same driving operation as in FIG. 12A (FIG. 8A) is performed except that the  
5 light-shielded pixel power supply line 10 is fixed to the GND potential.

First, a pixel output select signal  $\phi\text{SEL1}$  is set to "H" level to connect amplification MOS transistors M321 and M331 to vertical signal lines V2 and V3 and  
10 current sources I42 and I43 through row select MOS transistors M421 and M431. On the other hand, a vertical signal line V1 is fixed to GND because there is no current path flowing to a pixel current source I41. Before the read of optical signal charges from  
15 photodiodes D11 to D31, a pixel reset signal  $\phi\text{RS1}$  is set to "H" level to reset the gates of the amplification MOS transistors M321 and M331 to the effective pixel power supply line 7 through reset MOS transistors M221 and M231.

20 On the other hand, the gate potential of an amplification MOS transistor M311 is set to the GND potential. The potential is fixed to GND because the light-shielded pixel power supply line 10 is disconnected from the vertical signal line V1, and  
25 there is no current path flowing to the pixel current source I41.

Next, the pixel reset signal  $\phi\text{RS1}$  is returned to

"L" level to disconnect the effective pixel power supply line 7 from the gates of the amplification MOS transistors M311 to M331. Subsequently, the reset signal sample control signal  $\phi_{SHR}$  is set to "H" level to store the reset signal components of the vertical signal lines V2 and V3 in reset signal capacitors CSHR2 and CSHR3 through reset signal switches M42 and M43 and the GND component of the vertical signal line V1 in a reset signal capacitor CSHR1 through a reset signal switch M41. After the end of storage in the reset signal capacitors CSHR1 to CSHR3, the reset signal sample control signal  $\phi_{SHR}$  is returned to "L" level to cause the reset signal capacitors CSHR2 and CSHR3 to hold the stored reset signal components and the reset signal capacitor CSHR1 to hold the GND component.

After that, a PD signal transfer signal  $\phi_{TR1}$  is set to "H" level to transfer the optical signal charges in the photodiodes D21 and D31 to the gates of the amplification MOS transistors M321 and M331 through transfer MOS transistors M121 and M131.

On the other hand, the optical signal charges in the photodiode D11 cannot be transferred because the gate potential of the amplification MOS transistor M311 is GND. The potential remains almost GND.

After the end of transfer, the PD signal transfer signal  $\phi_{TR1}$  is returned to "L" level to disconnect the photodiodes D11 to D31 from the gates of the

amplification MOS transistors M311 to M331.

Subsequently, the optical signal sample control signal  $\phi$ SHS is set to "H" level to store the optical signal components of the vertical signal lines V2 and V3 in optical signal capacitors CSHS2 and CSHS3 through optical signal switches M52 and M53 and the GND component of the vertical signal line V1 in an optical signal capacitor CSHS1 through an optical signal switch M51. After the end of storage in the optical signal capacitors CSHS1 to CSHS3, the optical signal sample control signal  $\phi$ SHS is returned to "L" level to cause the optical signal capacitors CSHS2 and CSHS3 to hold the stored optical signal components and the optical signal capacitor CSHS1 to hold the GND component. Finally, column select signals  $\phi$ H1 to  $\phi$ H3 from a horizontal scanning circuit 5 are sequentially set to "H" level. Accordingly, the voltages held in the reset signal capacitors CSHR1 to CSHR3 and optical signal capacitors CSHS1 to CSHS3 are read out to a differential circuit 9 through horizontal select switches M61 to M63 and M71 to M73.

The differential circuit 9 obtains the difference between each reset signal component and a corresponding optical signal component and sequentially outputs the difference to a sensor output line OUT.

The read of the pixel cells connected to the first row is thus completed. At this time, both the reset

signal capacitor CSHR1 and the optical signal capacitor CSHS1 hold the GND component. For this reason, the output from the differential circuit 9 is zero.

5       The signal output levels of effective pixels PIX21 and PIX31 are corrected on the basis of the zero output from the differential circuit 9. In the same way as described above, the signals of the pixel cells connected to the second and subsequent rows are sequentially read out in accordance with signals from a  
10       vertical scanning circuit 3 so that the read of all pixel cells is ended.

      As described above, in the sixth embodiment, when very strong light such as a spotlight or sunlight is incident, a reference signal level different from the  
15       signal components of light-shielded pixels PIX11 to PIX13 is output. With this arrangement, an image which is not influenced by a black level variation observed in the light-shielded pixels PIX11 to PIX13 can be obtained. In addition, one control line for the noise  
20       suppressing circuit 4 is added to change the drive timing. This change makes it possible to select whether the signal components from the light-shielded pixels PIX11 to PIX13 or the reference signal level is to be output. Hence, the increase in chip area can be  
25       minimized. Furthermore, it is unnecessary to output both the output levels of the light-shielded pixels PIX11 to PIX13 and the reference signal level different



from the output data of the light-shielded pixels PIX11 to PIX13. For this reason, the time necessary for the read on the entire screen can be shortened. In addition, any degradation in characteristic due to power supply noise, GND noise, and the like can be suppressed by executing differential processing.  
(Seventh Embodiment)

A solid-state image sensing apparatus according to the seventh embodiment of the present invention has the same arrangement as in FIG. 1 described above. The same reference numerals as in FIG. 1 denote the same constituent elements in the seventh embodiment, and different operations will mainly be described below by appropriately referring to FIG. 1.

FIG. 13A is a timing chart showing the read operation for an output signal from a light-shielded pixel unit 1, which is used when the incident light amount is small, in the solid-state image sensing apparatus according to the seventh embodiment of the present invention. The drive timing is the same as in FIG. 2A, and repetitive description will be omitted.

The read operation for a reference signal different from the output from the light-shielded pixel unit 1, which is used when very strong light such as a spotlight or sunlight is incident, in the solid-state image sensing apparatus according to the seventh embodiment of the present invention will be described

next in detail with reference to the timing chart shown in FIG. 13B. The operation until CDS1 to CDS3 of a noise suppressing circuit 4 are caused to hold the pixel signal components of a light-shielded pixel PIX11 and effective pixels PIX21 and PIX31 is the same as in FIG. 13A (FIG. 2A). After that, a horizontal scanning circuit 5 fixes a column select signal  $\phi H1$  to "L" level and sequentially sets column select signals  $\phi H2$  and  $\phi H3$  to "H" level. Accordingly, the reset level of an output amplifier 6, and subsequently, the pixel signal components of the effective pixels PIX21 and PIX31, which are stored in the noise suppressing circuit 4, are read out through horizontal select switches M32 and M33 in the time-series order and output through the output amplifier 6. At this time, in the seventh embodiment, the signal output levels of the effective pixels PIX21 and PIX31 are corrected on the basis of the reset level of the output amplifier 6, which is different from the pixel signal component of the light-shielded pixel PIX11.

As described above, in the seventh embodiment, when very strong light such as a spotlight or sunlight is incident, a reference signal component different from the signal components of the light-shielded pixels PIX11 to PIX13 is output. With this arrangement, an image which is not influenced by a black level variation observed in the light-shielded pixels PIX11

to PIX13 can be obtained. In addition, it is unnecessary to output both the output levels of the light-shielded pixels PIX11 to PIX13 and the reference signal level different from the output data of the light-shielded pixels PIX11 to PIX13. For this reason, the time necessary for the read on the entire screen can be shortened.

(Eighth Embodiment)

The arrangement of a solid-state image sensing apparatus according to the eighth embodiment of the present invention is different from FIG. 9 described above in that a single power supply line 7 is commonly used as a light-shielded pixel power supply line 10 which supplies a power to a light-shielded pixel unit 1 and an effective pixel power supply line 7 which supplies power to an effective pixel unit 2. The remaining parts are the same as in FIG. 9. The same reference numerals as in FIG. 9 denote the same constituent elements in the eighth embodiment, and different operations will mainly be described below by appropriately referring to FIG. 9.

FIG. 14A is a timing chart showing the read operation for the output signal from the light-shielded pixel unit 1, which is used when the incident light amount is small, in the solid-state image sensing apparatus according to the eighth embodiment of the present invention. The clamp control signal  $\phi_{CL}$  is set

to "H" level at the same timing as that of the clamp control signal  $\phi CL1$  in FIG. 4A. In this case, the drive timing is the same as in FIG. 4A, and repetitive description will be omitted.

5           The read operation for a reference signal different from the output from the light-shielded pixel unit 1, which is used when very strong light such as a spotlight or sunlight is incident, in the solid-state image sensing apparatus according to the eighth  
10           embodiment of the present invention will be described next in detail with reference to the timing chart shown in FIG. 14B. The operation until optical signal components are stored in sample-and-hold capacitors CSH1 to CSH3 is the same as in FIG. 13A (FIG. 4A).  
15           After that, a horizontal scanning circuit 5 fixes a column select signal  $\phi H1$  to "L" level and sequentially sets column select signals  $\phi H2$  and  $\phi H3$  to "H" level. Accordingly, the reset level of an output amplifier 6, and subsequently, the pixel signal components of  
20           effective pixels PIX21 and PIX31, which are stored in a noise suppressing circuit 4, are read out through horizontal select switches M32 and M33 in the time-series order and output through the output amplifier 6. At this time, the signal output levels of  
25           the effective pixels PIX21 and PIX31 are corrected on the basis of the reset level of the output amplifier 6, which is different from the pixel signal component of a

light-shielded pixel PIX11. In the same way as described above, the signals of the pixel cells connected to the second and subsequent rows are sequentially read out in accordance with row select signals from a vertical scanning circuit 3 so that the read of all pixel cells is ended.

As described above, in the eighth embodiment, when very strong light such as a spotlight or sunlight is incident, a reference signal level different from the signal components of light-shielded pixels PIX11 to PIX13 is output. With this arrangement, an image which is not influenced by a black level variation observed in the light-shielded pixels PIX11 to PIX13 can be obtained. In addition, the drive timing of the horizontal scanning circuit 5 is changed. This change makes it possible to select whether the signal components from the light-shielded pixels PIX11 to PIX13 or the reference signal level is to be output. Hence, the chip area does not increase. Furthermore, it is unnecessary to output both the output levels of the light-shielded pixels PIX11 to PIX13 and the reference signal level different from the output data of the light-shielded pixels. For this reason, the time necessary for the read on the entire screen can be shortened.

(Ninth Embodiment)

The arrangement of a solid-state image sensing

apparatus according to the ninth embodiment of the present invention is different from that shown in FIG. 7 described above in that the gate of an optical signal switch M51 is connected to an optical signal sample control signal  $\phi$ SHS1. The remaining parts are the same as in FIG. 7. The same reference numerals as in FIG. 7 denote the same constituent elements in the ninth embodiment, and different operations will mainly be described below by appropriately referring to FIG. 7.

FIG. 15A is a timing chart showing the read operation for the output signal from a light-shielded pixel unit 1, which is used when the incident light amount is small, in the solid-state image sensing apparatus according to the ninth embodiment of the present invention. A reset signal sample control signal  $\phi$ SHR is set to "H" level at the same timing as that of the reset signal sample control signal  $\phi$ SHR1 in FIG. 8A. In this case, the drive timing is the same as in FIG. 8A, and repetitive description will be omitted.

The read operation for a reference signal different from the output from the light-shielded pixel unit 1, which is used when very strong light such as a spotlight or sunlight is incident, in the solid-state image sensing apparatus according to the ninth embodiment of the present invention will be described next in detail with reference to the timing chart shown

in FIG. 15B. The operation until reset signal components are stored in reset signal capacitors CSHR1 to CSHR3 and optical signal components are stored in optical signal capacitors CSHS1 to CSHS3 is the same as in FIG. 15A (FIG. 8A).

After that, a horizontal scanning circuit 5 fixes a column select signal  $\phi H1$  to "L" level and sequentially sets column select signals  $\phi H2$  and  $\phi H3$  to "H" level. Accordingly, the reset level of a differential circuit 9, and subsequently, the voltages held in the reset signal capacitors CSHR2 and CSHR3 and optical signal capacitors CSHS2 and CSHS3 of a noise suppressing circuit 4 are read out to the differential circuit 9 through horizontal select switches M62 and M63 and M72 and M73. The differential circuit 9 obtains the difference between each reset signal component and a corresponding optical signal component and sequentially outputs the difference to a sensor output line OUT. The read of the pixel cells connected to the first row is thus completed. In the ninth embodiment, the signal output levels of effective pixels PIX21 and PIX31 are corrected on the basis of the reset level of the differential circuit 9.

In the same way as described above, the signals of the pixel cells connected to the second and subsequent rows are sequentially read out in accordance with signals from a vertical scanning circuit 3 so that the

read of all pixel cells is ended.

As described above, in the ninth embodiment, when very strong light such as a spotlight or sunlight is incident, a reference signal level different from the signal components of light-shielded pixels PIX11 to PIX13 is output. With this arrangement, an image which is not influenced by a black level variation observed in the light-shielded pixels PIX11 to PIX13 can be obtained. In addition, the drive timing of the horizontal scanning circuit 5 is changed. This change makes it possible to select whether the signal components from the light-shielded pixels PIX11 to PIX13 or the reference signal level is to be output. Hence, the chip area does not increase. Furthermore, it is unnecessary to output both the output levels of the light-shielded pixels PIX11 to PIX13 and the reference signal level different from the output data of the light-shielded pixels PIX11 to PIX13. For this reason, the time necessary for the read on the entire screen can be shortened. In addition, any degradation in characteristic due to power supply noise, GND noise, and the like can be suppressed by executing differential processing.

The relationship between appended claims and the above-described first to ninth embodiments is as follows. An effective signal photoelectric conversion unit in claims corresponds to the effective pixel unit



2. A reference signal photoelectric conversion unit corresponds to the light-shielded pixel unit 1. A noise suppressing unit corresponds to the noise suppressing circuit 4. A switch unit corresponds to the clamp switch. A first power supply line corresponds to the pixel power supply line 7. A second power supply line corresponds to a light-shielded pixel power supply line 10.

(10th Embodiment)

The 10th embodiment in which one of the solid-state image sensing apparatuses according to the above-described first to ninth embodiments is applied to a camera will be described below in detail.

FIG. 16 is a block diagram showing the arrangement of the camera according to the 10th embodiment of the present invention.

As shown in FIG. 16, a photographing lens 30 and shutter/stop 29 are arranged on the optical path of object light. An imager 21 is arranged on the imaging plane of light that has passed through the shutter/stop 29. The imager 21 corresponds to the solid-state image sensing apparatus according to one of the above-described first to ninth embodiments.

The output from the imager 21 is connected to the inputs of an image processing unit 23 and luminance information acquisition unit 24 through a CDS · A/D 22. The output from the luminance information acquisition

unit 24 is connected to the input of a timing generator (imager control unit) 25 through an OB/dummy switching determination unit 26 such as a CPU.

5       Outputs from the timing generator 25 are connected to the inputs of the imager 21 and CDS·A/D 22. In addition, the output from an exposure control unit 27 and that from a photometry unit 28 are connected to the inputs of the OB/dummy switching determination unit 26.

10       A determination unit in claims corresponds to the OB/dummy switching determination unit 26.

      In this arrangement, the shutter/stop 29 is driven and controlled by the exposure control unit 27. An analog video signal is output from the imager 21 exposed through the photographing lens 30 and  
15       shutter/stop 29 to the CDS·A/D 22.

      The analog video signal contains a light-receiving pixel signal and a light-shielded pixel signal or reference signal level. The analog video signal is digitized by correlated double sampling and analog-to-  
20       digitized conversion by the CDS·A/D 22. At this time, the black level is fed back and clamped in the camera by using the light-shielded pixel signal or reference signal level selectively output from the imager 21. The output signal from the CDS·A/D 22 is subjected to  
25       3-CCD processing, spatial frequency band correction, and YCC processing by the image processing unit 23 and output to a recording medium or monitor (not shown).

The output signal from the CDS·A/D 22 is also input to the luminance information acquisition unit 24. The luminance information acquisition unit 24 generates an evaluation value of luminance information and inputs it to the OB/dummy switching determination unit 26. The evaluation value of luminance information is obtained in the following way. For example, on an erect object image shown in FIG. 17, luminance level equivalent signals are added and averaged for each divided area. The maximum value of the obtained values is used as the evaluation value. Shutter speed information and stop information in exposure control are input from the exposure control unit 27 to the OB/dummy switching determination unit 26. Object luminance information is also input to the OB/dummy switching determination unit 26 from the photometry unit 28 which measures the luminance of the object (not shown). The imager 21 receives a driving pulse and a control signal necessary for switching of light-shielded pixel signal/reference signal from the timing generator 25. A signal representing the timing of sampling the analog video signal and a signal representing the black level clamp operation period are input from the timing generator 25 to the CDS·A/D 22. The OB/dummy switching determination unit 26 sends an instruction signal for an operation mode including switching of light-shielded pixel signal/reference signal.

The first operation example of the camera according to the 10th embodiment of the present invention will be described below in detail with reference to the flowchart shown in FIG. 18.

5           When the first operation starts, the reference signal (instruction signal) is selectively output from the OB/dummy switching determination unit 26 to the timing generator 25 (step S1). The exposure control unit 27 executes exposure control (step S2). The  
10           timing generator 25 is operated to cause the imager 21 to output an analog video signal of one frame. The CDS·A/D 22 digitizes the analog video signal (step S3). The luminance information acquisition unit 24 generates an evaluation value of luminance information in the  
15           above-described way (step S4). The OB/dummy switching determination unit 26 determines in the above-described way whether a high-luminance area exists (step S5). If YES in step S5, the reference signal is selectively output from the OB/dummy switching determination unit  
20           26 to the timing generator 25 (step S6). If NO in step S5, the light-shielded pixel signal is selectively output from the OB/dummy switching determination unit 26 to the timing generator 25 (step S7). The exposure control unit 27 executes exposure control (step S8).  
25           The timing generator 25 is operated to cause the imager 21 to output an analog video signal of one frame. The CDS·A/D 22 digitizes the video signal (step S9). The

image processing unit 23 executes image processing (step S10). The above operation is executed for each frame.

The first operation is thus ended.

5           The second operation example of the camera according to the 10th embodiment of the present invention will be described next in detail with reference to the flowchart shown in FIG. 19.

10           When the second operation starts, the photometry unit 28 acquires object luminance information on the basis of a photographing instruction from an operation unit (not shown) (step S11). The OB/dummy switching determination unit 26 determines whether a high-luminance area exists (step S12).

15           If YES in step S12, the reference signal is selectively output from the OB/dummy switching determination unit 26 to the timing generator 25 (step S13). If NO in step S12, the light-shielded pixel signal is selectively output from the OB/dummy switching determination unit 26 to the timing generator 25 (step S14).

20

          The exposure control unit 27 executes exposure control (step S15). The timing generator 25 is operated to cause the imager 21 to output a video signal of one frame. The CDS·A/D 22 digitizes the video signal (step S16). The image processing unit 23 executes image processing (step S17). The above

25

operation is executed for each frame. The second operation is thus ended.

As described above, in the 10th embodiment, when very strong light such as a spotlight or sunlight is incident, a reference signal different from a light-shielded pixel signal is output. With this arrangement, an image which is not influenced by a black level variation observed in the light-shielded pixels can be obtained. In addition, the time necessary for the read on the entire screen can be shortened. Furthermore, any degradation in characteristic due to power supply noise or GND noise can be suppressed by executing differential processing. In addition, satisfactory video signal processing and iris control are implemented.

The first to tenth embodiments of the present invention have been described above. The present invention is not limited to these embodiments, and various changes and modifications can be made without departing from the spirit and scope of the present invention. For example, a plurality of light-shielded pixel units may be arranged in a plurality of rows. In this case, since the influence of fixed pattern noise can further be reduced, the reliability of the reference signal level for correction further increases.

According to the present invention, a solid-state

image sensing apparatus which can appropriately correct the black level of a video signal even when a high-luminance state or spotlight exists can be provided.

5           Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details, representative devices, and illustrated examples shown and described herein.

10         Accordingly, various modifications may be made without departing from the spirit or scope of the general inventive concept as defined by the appended claims and their equivalents.